1. An active pixel sensor, comprising:

a p type epitaxial silicon substrate;

an N well formed in said substrate;

a P well formed in said N well;

a deep N well formed in said substrate beneath said P well;

an overlap region formed between said N well and said deep N well wherein said overlap region electrically connects said N well to said deep N well when said overlap region is not depleted of charge carriers and electrically isolates said N well from said deep N well when said overlap region is depleted of charge carriers;

a first N region and a second N region formed in said P well; and

a P region formed in said N well.

2. The active pixel sensor of claim 1 wherein said first N region and said second N region provide electrical communication to said P well and said P region provides electrical communication to said N well.

3. The active pixel sensor of claim 1 wherein the potential of said P well and the potential of said N well determine whether or not said overlap region is depleted of charge carriers or is not depleted of charge carriers.

4. The active pixel sensor of claim 1 wherein said first N region, said second N region, and said P well can be used to form a floating gate field effect transistor.

5. The active pixel sensor of claim 1 wherein the potential of said P well is set so that said overlap region is depleted of charge carriers during a charge integration period.

6. The active pixel sensor of claim 1 wherein the potential of said P well is set so that said overlap region is not depleted of charge carriers after a charge integration period has been completed.

7. The active pixel sensor of claim 1 wherein the potential of said P well is set so that said overlap region is not depleted of charge carriers after a charge integration period has been completed and said first N region, said second N region, and said P well are used as a floating gate field effect transistor.

8. An array if active pixel sensors comprising:

a p type epitaxial silicon substrate;

a number of N wells formed in said substrate;

a P well formed in each of said N wells;

a deep N well formed in said substrate wherein said deep N well extends beneath each of said P wells;

an overlap region formed between each of said N wells and said deep N well wherein said each of said overlap regions electrically connects one of said N wells to said deep N well when that said overlap region between that said N well and said deep N well is not depleted of charge carriers and electrically isolates one of said N wells from said

deep N well when that said overlap region between that said N well and said deep N well is not depleted of charge carriers;

a first N region and a second N region formed in each of said P wells; and

a P region formed in each of said N wells.

9. The array of claim 8 wherein said first N region and said second N region in each of said P wells provide electrical communication to that said P well.

10. The array of claim 8 wherein said P region formed in each of said N wells provides electrical communication to that said N well.

11. The array of claim 8 wherein for each of said N wells the potential of that said N well and the potential of said P well in that said N well determines whether or not said overlap region between that said N well and said deep N well is depleted of charge carriers or is not depleted of charge carriers.

12. The array of claim 8 wherein for each of said N wells said P well in that said N well, said first N region in said P well in that said N well, and said second N region in said P well in that said N well can be used to form a floating gate field effect transistor in that said N well.

13. The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are not depleted of charge carriers during a reset cycle.

14. The array of claim 8 wherein a selected group of said N wells can be binned together by setting the potentials of each of said P wells in said selected group of said N wells so that said overlap regions between each of said N wells in said selected group of said N wells and said deep N well are not depleted of charge.

15. The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are depleted of charge carriers during a charge integration cycle.

16. The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are not depleted of charge carriers after a charge integration cycle has been completed.

17. The array of claim 8 wherein the potentials of each of said P wells are set so that said overlap regions between each of said N wells and said deep N well are not depleted of charge carriers after a charge integration cycle has been completed and said first N region, said second N region, and said P well in each of said N wells are used as a floating gate field effect transistor.

18. An active pixel sensor, comprising:

an n type epitaxial silicon substrate;

a P well formed in said substrate;

an N well formed in said P well;

a deep P well formed in said substrate beneath said N well;

an overlap region formed between said P well and said deep P well wherein said overlap region electrically connects said P well to said deep P well when said overlap region is not depleted of charge carriers and electrically isolates said P well from said deep P well when said overlap region is depleted of charge carriers;

a first P region and a second P region formed in said N well; and

an N region formed in said P well.

19. The active pixel sensor of claim 18 wherein said first P region and said second P region provide electrical communication to said N well and said N region provides electrical communication to said P well.

20. The active pixel sensor of claim 18 wherein the potential of said N well and the potential of said P well determine whether or not said overlap region is depleted of charge carriers or is not depleted of charge carriers.

21. The active pixel sensor of claim 18 wherein said first P region, said second P region, and said N well can be used to form a floating gate field effect transistor.

22. The active pixel sensor of claim 18 wherein the potential of said N well is set so that said overlap region is depleted of charge carriers during a charge integration period.

23. The active pixel sensor of claim 18 wherein the potential of said N well is set so that said overlap region is not depleted of charge carriers after a charge integration period has been completed.

24. The active pixel sensor of claim 18 wherein the potential of said N well is set so that said overlap region is not depleted of charge carriers after a charge integration period has been completed and said first P region, said second P region, and said N well are used as a floating gate field effect transistor.

25. An array if active pixel sensors comprising:

an n type epitaxial silicon substrate;

a number of P wells formed in said substrate;

an N well formed in each of said P wells;

a deep P well formed in said substrate wherein said deep P well extends beneath each of said N wells;

an overlap region formed between each of said P wells and said deep P well wherein said each of said overlap regions electrically connects one of said P wells to said deep P well when that said overlap region between that said P well and said deep P well is not depleted of charge carriers and electrically isolates one of said P wells from said

deep P well when that said overlap region between that said P well and said deep P well is not depleted of charge carriers;

a first P region and a second P region formed in each of said N wells; and

an N region formed in each of said P wells.

26. The array of claim 25 wherein said first P region and said second P region in each of said N wells provide electrical communication to that said N well.

27. The array of claim 25 wherein said P region formed in each of said P wells provides electrical communication to that said P well.

28. The array of claim 25 wherein for each of said P wells the potential of that said P well and the potential of said N well in that said P well determines whether or not said overlap region between that said P well and said deep P well is depleted of charge carriers or is not depleted of charge carriers.

29. The array of claim 25 wherein for each of said P wells said N well in that said P well, said first P region in said N well in that said P well, and said second P region in said N well in that said P well can be used to form a floating gate field effect transistor in that said P well.

30. The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are not depleted of charge carriers during a reset cycle.

31. The array of claim 25 wherein a selected group of said P wells can be binned together by setting the potentials of each of said N wells in said selected group of said P wells so that said overlap regions between each of said P wells in said selected group of said P wells and said deep P well are not depleted of charge.

32. The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are depleted of charge carriers during a charge integration cycle.

33. The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are not depleted of charge carriers after a charge integration cycle has been completed.

34. The array of claim 25 wherein the potentials of each of said N wells are set so that said overlap regions between each of said P wells and said deep P well are not depleted of charge carriers after a charge integration cycle has been completed and said first P region, said second P region, and said N well in each of said P wells are used as a floating gate field effect transistor.